

WHAT IS CLAIMED IS:

- 1 1. A method of forming a semiconductor varactor device having improved linearity
2 comprising the steps of:
 - 3 providing a semiconductor substrate;
 - 4 forming at least a first and a second differential varactor element on said semiconductor
 - 5 substrate, the forming of each of said differential varactor elements comprising the steps of
 - 6 forming first, second and third N+ doped regions in an N well, forming a first gate for
 - 7 controlling said first and second N+ doped regions and forming a second gate for controlling said
 - 8 second and third N+ doped regions;
 - 9 connecting said first, second and third N+ doped regions of said first differential varactor
 - 10 element to receive power having a first voltage; and
 - 11 connecting said first, second and third N+ doped regions of said second differential
 - 12 varactor element to receive power having a second voltage different than said first voltage.
- 1 2. The method of claim 1 further comprising forming a first resistor in said semiconductor
2 varactor device connected to receive power from a voltage source, and wherein said step of
3 connecting said first, second and third N+ doped regions of said first differential varactor
4 comprises connecting to said voltage source, and wherein said step of connecting said first,
5 second and third N+ doped regions of said second differential varactor comprises connecting to
6 said voltage source through said first resistor.
- 1 3. The method of claim 1 wherein said step of forming said first and second gates comprises
2 the step of forming a first N-type gate and forming a second N-type gate.

1 4. The method of claim 2 wherein said step of forming a first resistor comprises the step of
2 forming another resistor and said first resistor and wherein said another resistor is connected in
3 series and between said voltage source and said first resistor, wherein said step of connecting
4 said first, second and third N+ doped regions of said first differential varactor element to receive
5 power from said voltage source comprises the step of connecting said regions to said voltage
6 source through said another resistor, and such that said second differential varactor elements
7 receive power from said voltage source through both of said another and said first resistors.

1 5. The method of claim 2 wherein said step of forming at least a first and a second
2 differential varactor element comprises the step of forming at least a first, a second and a third
3 differential varactor element, wherein said step of forming a first resistor comprises the step of
4 forming first and second resistors connected in series and further comprising the step of
5 connecting said first, second and third N+ doped regions of said third differential varactor
6 element to receive power from said voltage source through both of said first and second resistors.

1 6. The method of claim 5 wherein said step of forming first and second resistors comprises
2 the step of forming another resistor and said first and second resistors and wherein said another
3 resistor is connected in series between said voltage source and said first and second resistors and
4 wherein said step of connecting said first, second and third N+ doped regions of said first
5 differential varactor element to receive power from said voltage source comprises the step of
6 connecting said voltage source to said regions only through said another resistor.

1 7. The method of claim 2 wherein said step of forming first and second differential varactor
2 elements comprises the step of forming a plurality of differential varactor elements, wherein said
3 step of forming a first resistor comprises the step of forming a plurality of resistors connected in

4 series such that nodes are defined between adjacent ones of said serially connected plurality of
5 resistors and further comprising the step of connecting said first, second and third N+ doped
6 regions of one each of said plurality of differential varactor elements to one each of said nodes
7 such that said first, second and third N+ doped regions of different ones of said plurality of
8 differential varactor elements are electrically separated by one of said plurality of resistors.

1 8. The method of claim 7 wherein said step of forming a plurality of resistors further
2 comprises the step of forming said plurality of resistors and another resistor and connecting said
3 another resistor in series between said voltage source and said serially connected plurality of
4 resistors and wherein said step of connecting said first differential varactor element to receive
5 power from said voltage source comprises the step of connecting said voltage source to said
6 varactor element through said another resistor.

1 9. The method of claim 1 further comprising the steps of connecting said first gate of said
2 first and second differential varactor elements together at a first terminal and connecting said
3 second gate of said first and second differential varactor elements together at a second terminal.

1 10. The method of claim 5 further comprising the steps of connecting said first gate of said
2 first, second and third differential varactor elements together at a first terminal and connecting
3 said second gate of said first, second and third differential varactor element together at a second
4 terminal.

1 11. The method of claim 7 further comprising the steps of connecting said first gate of said
2 plurality of differential varactor elements together at a first terminal and connecting said second
3 gate of said plurality of differential varactor elements together at a second terminal.

1 12. The method of claim 9 further comprising connecting said first and second terminals to
2 an oscillator circuit as a voltage controlled capacitor.

1 13. The method of claim 11 further comprising connecting said first and second terminals to
2 an oscillator circuit as a voltage controlled capacitor.

1 14. The method of claim 1 wherein said forming steps are according to a CMOS process.

1 15. The method of claim 9 wherein said first and second gates are N-type gates.

1 16. The method of claim 10 wherein said first and second gates are N-type gates.

1 17. The method of claim 11 wherein said first and second gates are N-type gates.

1 18. The method of claim 1 further comprising the steps of forming another differential
2 varactor element on said semiconductor, said another differential varactor element comprising
3 first, second and third P+ doped regions in a P well, a first gate for controlling said first and
4 second P+ doped regions and a second gate for controlling said second and third P+ doped
5 regions, and connecting said first, second and third P+ doped regions to receive power from said
6 voltage source.

1 19. The method of claim 2 wherein said step of forming a first resistor comprises the step of
2 forming said first resistor from a polysilicon material.

1 20. A semiconductor varactor device having improved linearity and suitable for being
2 manufactured by a standard CMOS process comprising:

3 a semiconductor substrate;

4 at least two N wells formed in said semiconductor substrate;

5 first, second and third N+ doped regions formed in each of said at least two N wells;

6 a first gate connected to a first junction and formed between said first and second N+

7 doped regions of a first one of said at least two N wells, and a first gate connected to said first

8 junction and formed between said first and second N+ doped regions of the other one of said at

9 least two N wells;

10 a second gate connected to a second junction and formed between said second and third

11 N+ doped regions of said first one of said at least two N wells and a second gate connected to

12 said second junction and formed between said second and third N+ doped regions of said other

13 one of said at least two N wells; and

14 a power source for providing a first voltage level and a second voltage level, said power

15 source connecting said first resistor and said first, second and third N+ doped regions formed in

16 said first one of said at least two N wells to receive power having said first voltage level and

17 connecting said first, second and third N+ doped regions formed in said second one of said at

18 least two N wells to receive power having said second voltage level.

1 21. The semiconductor varactor of claim 20 wherein said first voltage level is the output of

2 said power source, and further comprising a first resistor formed on said semiconductor substrate

3 and having a first end and a second end, said first end connected to the output of said power

4 source and said second end connected to said first, second and third N+ doped regions formed in

5 said second of said at least two N wells to provide said second voltage level.

1 22. The semiconductor varactor of claim 20 wherein said first and second gates are N-type
2 gates.

1 23. The semiconductor varactor of claim 21 further comprising another resistor connected in
2 series with said first resistor, said another resistor further connected between said voltage source
3 and said first resistor such that said first, second and third N+ doped regions formed in said first
4 one of said at least two N wells receives power from said voltage source through said another
5 resistor.

1 24. The semiconductor varactor of claim 21 wherein said at least two N wells comprise at
2 least three N wells and further comprising another first gate connected to said first junction and
3 formed between said first and second N+ doped regions of the third one of said at least three N
4 wells, another second gate connected to said second junction and formed between said second
5 and third N+ doped regions of the third one of said at least three N wells, a second resistor
6 connected in series with said first resistor and said first, second and third N+ doped regions of
7 the third one of said at least three N wells connected to receive power from said voltage source
8 through said first and second resistors.

1 25. The semiconductor varactor of claim 24 further comprising another resistor connected in
2 series with said first and second resistor, said another resistor further connected between said
3 voltage source and said first resistor such that said first, second and third N+ doped regions
4 formed in said first one of said at least three N wells receives power from said voltage source
5 through said another resistor.

1 26. The semiconductor varactor of claim 21 wherein said at least two N wells comprise a
2 plurality of N wells, and further comprising a plurality of first gates connected to said first
3 junction and formed between said first and second N+ doped regions of said plurality of N wells,
4 a plurality of second gates connected to said second junction and formed between said second
5 and third N+ doped region of said plurality of N wells, a plurality of resistors connected in series
6 such that nodes are defined between two adjacent ones of said plurality of resistors, and wherein
7 said first, second and third N+ doped regions of each one of said plurality of N wells are
8 connected to one each of said nodes such that said first, second and third N+ doped regions of
9 each one of said plurality are electrically separated by one of said plurality of resistors.

1 27. The semiconductor varactor of claim 26 further comprising another resistor connected in
2 series with said plurality of resistors, said another resistor further connected between said voltage
3 source and said plurality of resistors such that said first, second and third N+ doped regions
4 formed in said first one of said plurality of N wells receive power from said voltage source
5 through said another resistor.

1 28. The semiconductor varactor of claim 21 further comprising circuitry for forming an
2 oscillator circuit when connected with said semiconductor varactor, said first and second
3 junctions of said varactor device connected such that said semiconductor varactor operates as a
4 voltage controlled capacitor of said oscillator circuit.

1 29. The semiconductor varactor of claim 20 wherein said first resistor is made of a
2 polysilicon material.

1 30. The semiconductor varactor of claim 20 further comprising a P well formed in said
2 semiconductor substrate and first, second and third P+ doped regions formed in said P well, a
3 first gate for controlling said first and second P+ doped regions and a second gate for controlling
4 said second and third P+ doped regions, said first, second and third P+ doped regions connected
5 to receive power from said voltage source.